AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 20, and continuing to page 1, line 25, as follows:

It is often desired, and indeed sometimes required, that the delay can be varied by a control signal. Commonly, there is a desire for the delay to be a certain fraction of a period, or an integer multiple of such a fraction. In such cases, a Delay-Locked-Loop (DLL) is often used. Usually, a DLL is designed by means of active circuits, most commonly inverters. However, in such DLL[[:]]s, a fixed number, N, of delay cells is used, which means that only phase delays of M/N*360°, where 0<M<N, can be obtained.

Please amend the caption at page 1, line 28, as follows:

BRIEF SUMMARY ~~OF THE INVENTION~~

Please amend the paragraph beginning at page 2, line 1, and continuing to page 2, line 4, as follows:

This need is addressed by ~~the present invention in that it discloses~~ a delay-locked loop circuit with input means for a signal that is to be delayed, the input means comprising means for splitting said input signal into a first and a second branch.

Please amend the paragraphs beginning at page 2, line 25, and continuing to page 2, line 27, as follows:

Fig 2 schematically shows the principle behind a delay-locked loop according to ~~the invention~~an example embodiment, and

Fig 3 shows a more detailed drawing of a delay component of ~~the invention~~an example embodiment.

Please amend the caption at page 2, line 29, as follows:

~~EMBODIMENTS~~DETAILED DESCRIPTION

Please amend the paragraphs beginning at page 2, line 30, and continuing to page 3, line 7, as follows:

In order to facilitate the understanding of the present ~~invention~~technology, a known ~~kind of~~ delay-locked loop (DLL) circuit 100 is shown in Fig 1. The circuit 100 in fig 1 comprises first input means 110 for an input signal, ~~V_{in}~~I_{in}, which input means split the input signal into a first and a second input branch.

The signal in the first input branch of the DLL-circuit is input to a tunable delay component 120, which component thus also has an input possibility for the input of a control or tuning signal, said control signal controlling the delay to which the input signal ~~V_{in}~~ I_{in} is exposed.

Please amend the paragraphs beginning at page 3, line 25, and continuing to page 4, line 7, as follows:

The DLL of fig 1 can thus provide a phase delay of an input signal, with the phase delay being varied by means of a control signal. However, in contemporary such DLL[[:]]s, the most commonly used building block in the delay component are active circuits, usually inverters. The use of, for example, inverters in the DLL will limit the available delays to a certain number of discrete steps.

In fig 2, a DLL 200 according to the invention is shown, which overcomes this problem of known DLL[[:]]s.

The DLL 200 of the ~~invention~~example embodiment of Fig. 2, in similarity to earlier known DLL[[:]]s, comprises an input means 210 for a signal ~~V_{in}~~ I_{in} which is to be delayed. The input means 210 split the input signal into a first and a second branch, and the signal in the first branch is connected to a component 220 for delaying the signal

Please amend the paragraph beginning at page 5, line 15, and continuing to page 5, line 19, as follows:

The filtered output signal from the phase detector 250 is then used as input to a control means 230 for controlling the electrical distance which a signal passing through the delay line will have to cover. In this way, the electrical distance can be kept at a constant and desired value, regardless of the wavelength of the input signal ~~V~~$_{in}$I$_{in}$.

Please amend the paragraph beginning at page 5, line 31, and continuing to page 6, line 8, as follows:

In fig 3, a tunable delay line 220 as used in fig 2 is shown in more detail[~~:~~]. ~~a~~As mentioned previously, the delay line 220 is preferably a tunable ferroelectric delay line. Such a delay line can ~~consist~~ comprise~~of~~ the components shown in fig 3~~:a~~. An electrical conductor 305 is supported by a dielectric material 310 which is a ferroelectric material. The ferroelectric material in turn rests on a ground plane 315. The control signal to the control means 230 shown in fig 2 is connected so that it applies a voltage, V_{TUNE} between the conductor 305 and the ground plane 315, thereby altering the dielectric constant ε of the material 310, which causes the electrical distance to be covered by a wave through the component 220 to vary as desired.

Please amend the paragraph beginning at page 6, line 15, and continuing to page 6, line 23, as follows:

Some advantages of the ~~invention that might be mentioned are~~technology include the following:

- Since the circuit ~~of the invention~~ is passive, it ~~doesn't~~ does not interfere with the input signal, thus offering the possibility of using a modulated input signal.
- As a passive circuit, it ~~doesn't~~ does not consume power.
- The circuit ~~of the invention~~ offers a wide tuning range.
- The phase delay offered by the circuit ~~of the invention~~ can be chosen more or less arbitrarily, and changed over a continuous range.